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EXAMINER	
PARIKH, KALPIT	
ART UNIT	**PAPER NUMBER**
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/538,371	DUTTA, SANTANU	
	Examiner	Art Unit	
	Kalpit Parikh	2187	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 June 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

I. APPLICATION INFORMATION

The instant application having Application No. 10532371 has a total of 16 claims pending in the application; there are 3 independent claims and 13 dependent claims, all of which are ready for examination by the examiner.

Applicants' submission of replacement drawings, as presented in the provisional application, is acknowledged.

Examiner acknowledges Applicants' amendments to the claims.

II. REJECTIONS NOT BASED ON PRIOR ART

Claim Objections

1. **CLAIMS 12-16** objected to because of the following informalities: Claim 12 recites control logic configured to *facilitate* use of cache buffer as a circular buffer. It is not clear what manner of configuring may facilitate use of a buffer as a circular buffer and it appears the claim does not require using the buffer as a circular buffer. Clarification is respectfully requested.

III. REJECTIONS BASED ON PRIOR ART

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

   A person shall be entitled to a patent unless –

   (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. **CLAIMS 1 AND 7** rejected under 35 U.S.C. 102(b) as being anticipated by Brown et al. (US Pat No. 5916309).

As per claims 1 and 7 Brown et al. disclose a butter management system for providing a plurality of independent buffers for use by an application, the system comprising:

- a buffer memory (see FIG 1: 22 and also COL 3 LINES 40-45), and
- a controller operably coupled to the buffer memory (see FIG 3), the controller configured to partition the buffer memory into the plurality of independent buffers (see e.g., FIG 2: 'REC. BUFF. 1' and also COL 5 LINES 20) dependent upon a partition parameter received from the application that indicates a quantity of the plurality (see COL 4 LIENS 24-30),

  [A communication parameter is indicative of the quantity of the plurality because a communication parameter determines a quantity of the plurality.]
- wherein each buffer of the plurality of independent butters has a buffer-size that is an integer power of two, to facilitate circular access to the buffer (see COL 5 LINES 18-20).

  [Brown et al. disclose a controller receiving parameters that determine a partitioning of the communication buffer from a host (application) prior to data transfer.]

4. **CLAIMS 1,3-5, 7-8, 10, 12-13 AND 15** rejected under 35 U.S.C. 102(b) as being anticipated by Nogradi (US Pat no. 5974518).

As per claim 1, and 7 Nogradi discloses a butter management system for providing a plurality of independent buffers for use by an application, the system comprising:

- a buffer memory (see FIG 2: 24), and
- a controller operably coupled to the buffer memory (see FIG 2: 14), the controller configured to partition the buffer memory into the plurality of independent buffers (see e.g., FIG 2: 'BUFFER 1') dependent upon a partition parameter (COL 11 LINES 37-41: 'new

values for the number of buffers from the driver') received from the application (see FIG 2: 41) that indicates a quantity of the plurality (see COL 4 LIENS 24-30),

[Nogradi discloses an application to provide partition parameter and a controller to divide the memory accordingly.]

- wherein each buffer of the plurality of independent butters has a buffer-size that is an integer power of two (see COL 3 LINES 63: '64 Kbytes of address space' and COL 7 LINES 1-9: 'buffers must be the same size') , to facilitate circular access to the buffer.

As per claim 3 and 8, Nogradi discloses the buffer management system of claim 1,

- wherein the buffer sizes of independent buffers are equal (see COL 7 LINES 1-8).

As per claim 4, Nogradi discloses the buffer management system of claim 1,

- wherein the controller is further configured to allocate the plurality of independent buffers among a plurality of independent buffers among a plurality of source-destination paths (see FIG 1: 10, 12).

[Nogradi discloses a controller to allocate buffers for receiving and transmitting buffers for a network comprising a plurality of sources and plurality of destinations.]

As per claims 5 and 10, Nogradi discloses the integrated circuit of claim 1,

- wherein the controller is further configured to provide a write interface and a read interface to the application (see FIG 2: 26), the write interface receiving, from the application, an identification of data to be stored (see FIG 2: 'RD1') and an identification of a select buffer of the plurality of independent buffers to store the data (see COL 4 LINES 54-59) and
- translating the identification of the select buffer to an address corresponding to the select buffer (see COL 4 LINES 21-24: 'points to'), and the read interface receiving, from the application, the identification of the select buffer (see FIG 2: 'RD1'), and translating the

identification of the select buffer to an address corresponding to the select buffer (see COL 4 LINES 21-24: 'points to').

As per claim 12, Nogradi discloses an integrated circuit for providing a plurality of buffers for use by an application, the circuit comprising

- a buffer memory (see FIG 2: 24), and
- a controller that includes write control logic and read control logic (see FIG 2: 26), wherein the controller is configured to partition the buffer memory into the plurality of buffers based on a partition parameter that is provided to the controller by the application (see COL 11 39-41), each buffer of the plurality of buffers having a size that is an integer power of two (see COL 3 LINES 63: '64 Kbytes of address space' and COL 7 LINES 1-9: 'buffers must be the same size'), and
- the write control logic and read control logic are each configured to facilitate use of each buffer as a circular buffer (see COL 4 LINES 14-16).

As per claim 13, Nogradi discloses the integrated circuit of claim 12,

- wherein the buffer sizes of independent buffers are equal (see COL 7 LINES 1-8).

As per claim 15, Nogradi discloses the integrated circuit of claim 12,

- wherein the write control logic effects a storage of a data value to a select buffer of the plurality of buffers based an identification of the data value (see FIG 2: 'RD") and an identification of the select buffer by translating the identification of the select buffer into an address corresponding to the select buffer (see FIG 2: RD1→'BUFFER 1') at which the data is to be stored, and the read control logic effect a retrieval of the data value based on the identification of the select buffer (see FIG 2: '26').

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. **CLAIMS 1-2, 6-7, 9, 11-12, AND 16** rejected under 35 U.S.C. 103(a) as being unpatentable over Shemla et al. (US Pat No. 5809557) in view of Brown et al. (US Pat No. 5916309).

As per claim 1 and 7, Shemla et al. disclose a buffer management system, comprising:

- a buffer memory (see Shemla et al. FIG 1: 12), and
- a controller operably coupled to the buffer memory, the controller configured to (see Shemla et al. FIG 1: 10)
    - o partition the buffer memory into the plurality of independent buffers (see Shemla et al. FIG 2: 40),
    - o wherein each buffer of the plurality of independent buffers has a buffer-size that is an integer power of two, to facilitate circular-access to the buffer (see Shemla et al. FIG 2: 'FIFO 0')

      [Shemla et al. teach facilitating circular-access to the buffer because Shemla et al. teach the buffer size is a power of two.]

However, Shemla et al. do not expressly disclose the partitioning is

- dependent upon a partition parameter received from the application that indicates a quantity of the plurality

In the same field of endeavor, Brown et al. disclose partitioning a memory into a plurality of buffers

- dependent upon a partition parameter received from the application that indicates a quantity of the plurality (see Brown et al. ABSTRACT)

At the time of invention it would have bee obvious to a person of ordinary skill in the art to modify the circuit of Shemla et al. to partition a buffer based on a partition parameter provided to the controller as suggested by Brown et al. (see Brown et al. COL 3 LINES 39-45).

The suggestion/motivation for doing so would have been because Brown et al. disclose the method of dynamically partitioning the memory based on a parameter improves memory utilization (see Brown et al. COL 5 LINES 28-37).

Therefore it would have been obvious at the time of invention to modify the circuit of Shemla et al. to partition the memory based on a partitioning parameter as taught by Brown et al. for the benefit of improved memory utilization to arrive at the invention as specified in the claims.

As per claim 2, and 9, Shemla et al. in view of Brown et al. disclose the buffer management system of claim 1, wherein

- the controller is configured to include a circular-increment function that requires only an address-increment function (see Shemla et al. COL 3 LINES 44-46) and a bit-overwrite function to effect a circular-increment of a pointer to a select buffer of the plurality of independent buffers (see Shemla et al. COL 3 LINES 44-46 AND LINES 48-51)

  [Shemla et al. disclose a circular buffer because Shemla et al. disclose the pointers are incremented to access a next buffer location.]

As per claims 6 and 11, Shemla et al. in view of Brown et al. disclose the buffer management system of claim 1, wherein

- the buffer memory is addressed by an M-bit address (see Shemla et al. COL 3 LINE 20: 'WR_ADDR') each buffer of the plurality of independent buffers is indexed by an N-bit

index (see Shemla et al. COL 3 LINE 25: 'WR_SEL') that forms a set of N most-significant-bits of the M-bit address (see Shemla et al. COL 3 LINES 25-26: 'upper 3 bits'), and

- the size of each buffer is at least 2^{M-N} (see Shemla et al. FIG 2: 40)

As per claim 12, Shemla et al. disclose an integrated circuit for providing a plurality of independent buffers for use by an application, the circuit comprising

- a buffer memory (see Shemla et al. FIG 1: 12), and
- a controller (see Shemla et al. FIG 1: 10) that includes write control logic (see Shemla et al. FIG 1: 14 AND 22), and read control logic (see Shemla et al. FIG 1: 16 AND 24), wherein the controller is configured to
  - o partition the buffer memory into the plurality of buffers (see Shemla et al. FIG 2: 40), each buffer of the plurality of buffers having a size that is an integer power of two (see Shemla et al. FIG 1: 'FIFO 0'), and
  - o the write control logic and read control logic are each configured to facilitate use of each buffer as a circular buffer (see Shemla et al. COL 3 LINES 48-51)

    [Shemla et al. disclose the pointer values are incremented by one after each read or write. Incrementing in such a manner is construed to facilitate the use of each buffer as a circular buffer.]

However, Shemla et al. do not expressly disclose the partitioning of the buffer memory may be

- based on a partition parameter that is provided to the controller by the application

[Shemla et al. disclose partitioning the buffer into N partitions, however Shemla et al. do not expressly disclose the partitioning is based on a partition parameter provided to the controller.]

In the same field of endeavor, Brown et al. disclose partitioning a buffer

- based on a partition parameter that is provided to the controller (see Brown et al. COL 3 LINE 39-45: 'communication parameter')

Brown et al. and Shemla et al. are analogous art because they are from the same field of endeavor, namely memory access and control.

At the time of invention it would have bee obvious to a person of ordinary skill in the art to modify the circuit of Shemla et al. to partition a buffer based on a partition parameter provided to the controller as suggested by Brown et al. (see Brown et al. COL 3 LINES 39-45).

The suggestion/motivation for doing so would have been because Brown et al. disclose the method of dynamically partitioning the memory based on a parameter improves memory utilization (see Brown et al. COL 5 LINES 28-37).

Therefore it would have been obvious at the time of invention to modify the circuit of Shemla et al. to partition the memory based on a partitioning parameter as taught by Brown et al. for the benefit of improved memory utilization to arrive at the invention as specified in the claims.

As per claim 16, Shemla et al. disclose the buffer management system of claim 1, wherein

- the buffer memory is addressed by an M-bit address (see Shemla et al. COL 3 LINE 20: 'WR_ADDR') each buffer of the plurality of independent buffers is indexed by an N-bit index (see Shemla et al. COL 3 LINE 25: 'WR_SEL') that forms a set of N most-significant-bits of the M-bit address (see Shemla et al. COL 3 LINES 25-26: 'upper 3 bits'), and

- the size of each buffer is at least 2^{M-N} (see Shemla et al. FIG 2: 40)

3. **CLAIM 14** rejected under 35 U.S.C. 103(a) as being unpatentable over Shemla et al. (US Pat No. 5809557) in view of Brown et al. (US Pat No. 5916309) as applied to claim 12 above, and further in view of Fadivi-Ardekani et al. (US Pat No. 6496916).

As per claim 14, Shemla et al. the integrated circuit of claim 12, wherein

- the use of each buffer as a circular buffer requires circular-addressing, and the controller is configured to effect the circular-addressing via an incrementer that is configured to increment an address to the buffer memory (see Shemla et al. COL 3 LINES 46-51), and

However, Shemla et al. do not expressly disclose

- a bit masker that is configured to overwrite select bits of the address, corresponding to an index to the buffer within the buffer memory

[Shemla et al. disclose the upper bits of the write address are utilized as the index into the buffer, however Shemla et al. do not disclose masking the upper bits of the write address.]

In the same field of endeavor Fadivi-Ardekani et al. disclose a memory partitioning circuit wherein

- a bit masker that is configured to overwrite select bits of the address (i.e., the upper bits), corresponding to an index to the buffer within the buffer memory (see Fadivi-Ardekani et al. FIG 2 AND FIG 3).

Fadivi-Ardekani et al. and Shemla et al. are analogous art because they are from the same field of endeavor namely, memory partitioning.

At the time of invention it would have been obvious to a person of ordinary skill in the art to modify the addressing of Shemla et al. write mask the index bits (i.e., 'WR_SEL'

bits) of the WR_ADDR as suggested by Fadivi-Ardekani et al. (see Fadivi-Ardekani et al. FIG 2 AND COL 2 LINES 18-24).

The suggestion/motivation for doing so would have been because Fadivi-Ardekani et al. disclose the masking of the upper bits to address a partitioned memory improves memory access timing (see Fadivi-Ardekani et al. COL 2 LINES 12-15).

Therefore it would have been obvious at the time of invention to modify addressing mechanism of Shemla et al. to mask the index bits of Shemla et al. as suggested by Fadivi-Ardekani et al. for the benefit of improved access timing to arrive at the invention as specified in the claims.

IV. ACKNOWLEDGMENT OF ISSUES RAISED BY THE APPLICANT

The 102(b) rejection is withdrawn because Applicants' representative states the Rickard et al. do not disclose a control that receives a partition parameter from an application and to partition the memory in dependence thereof (see PAGE 7 ¶ 4).

The remarks filed August 17,2007 have been fully considered but they are not deemed persuasive with regard to the 103 rejection.

1st POINT OF DISCUSSION:

Applicants' representative alleges the combination of Shemla and Brown, as presented in the previous Office Action, is improper.

Applicants' representative submits that neither reference teaches or suggests that a dynamic allocation is possible in the hardware implementation of the Shemla reference.

Applicants' representative suggests that the circuit taught by Shemla is not capable of dynamically partitioning the memory and is not compatible with the partitioning parameter as

taught by Brown (see PAGE 9 ¶ 1) because Shemla discloses the partitioning is fixed at time of design (see REMARKS PAGE 8 ¶ 4).

Examiner respectfully disagrees. As a threshold matter, Examiner notes that the claims do not recite dynamic allocation/dynamic partitioning. It is not clear from the claims when the recited partitioning is preformed (e.g., during device operation, prior to receiving data, or during device design etc.).

Shemla discloses a buffer design dependent on a partition parameter. Brown et al. discloses dynamically partitioning a memory into a plurality of independent buffers based upon communication parameters received from a host improves performance (see Brown et al. COL 5 LINES 28-37). Brown et al. is relied upon to disclose the motivation/suggestion to modify Shemla et al. to partition a memory into a plurality of independent buffers based on a partition parameter.

Furthermore, Brown discloses the dynamic partitioning of a memory into a plurality of independent buffers based on a communication parameter received from an application prior to data communication is applicable to any packet oriented link protocol (see Brown et al. COL 7 LINES 12-25).

It is well known in the art that devices such as FPGA may be utilized to implement alterable designs.

V. CLOSING COMMENTS

RELEVANT ART CITED BY THE EXAMINER

The following prior art made of record and not relied upon is cited to establish the level of skill in the applicant's art and those arts considered reasonably pertinent to applicant's disclosure. See MPEP 707.05(c).

The following reference teaches a dynamic partitioning of data based on a partition parameter.

U.S. PATENT/PGPUB No.	RELEVANT PORTIONS
6181700	COL 6 LINES 19-34

The following reference teaches a circular buffer with programmable size/increment parameters.

U.S. PATENT/PGPUB No.	RELEVANT PORTIONS
5623621	FIG 1, FIG 2

STATUS OF CLAIMS IN THE APPLICATION

The following is a summary of the treatment and status of all claims in the application as recommended by M.P.E.P. ' 707.07(i):

Va. CLAIMS REJECTED IN THE APPLICATION

Per the instant office action, claims 1-16 have received a second action on the merits and are subject of a final office action.

For at least the above reasons it is the examiner's position that the applicant's claims are not in condition for allowance.

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

VI. **DIRECTION OF FUTURE CORRESPONDENCES**

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kalpit Parikh whose telephone number is (571) 270-1173. The examiner can normally be reached on MON THROUGH FRI 7:30 TO 5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Donald Sparks can be reached on (571) 272-4201. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Kalpit Parikh/

Kalpit Parikh
Examiner
Art Unit 2187

October 9, 2007

Brian R. Peugh
Primary Examiner
10/26/07